Concordia
UNIVERSITY

Course	Number	Section
Introduction to VLSI	ENCS 454	W

Examination	Date	Time	# of pages
Final	April 1996	3 Hours	4

Instructor(s)

Dr. A.J. Al-Khalili

Materials allowed: [ ] No [X] Yes (Please specify)

Calculators allowed: [ ] No [X] Yes

Students are allowed one double-sided crib sheet using size 10 font, without diagrams.

Special Instructions:

Attempt all questions. Show all steps clearly.
In all your designs use the NT CMOS process parameters provided.
Students are required to return question paper with exam booklet(s).

1. A CMOS inverter is implemented in NT CMOS process with Ln = Lp = 1.2μ and $W_p = \mu_r W_n$, W_n = 1.2μ. At implementation the gate of the n-transistor was over etched by 0.2μ from all sides. Determine amount of shift in the voltage transfer characteristics from the ideal.

(10 marks)

2. (a) Draw the mask combination that gives you the layout for a p-transistor. Mark each mask clearly.

(6 marks)

(b) What are the consequences of not grounding the n-transistor in an inverter?

(2 marks)

(c) What is CIF (Caltech Intermediate Form)?

(2 marks)

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3. (a) Implement a complementary CMOS gate that produces the function F,

$$F = [(\overline{A} + \overline{B})(\overline{C} + \overline{D} + \overline{E}) + \overline{F}]\,\overline{G}$$

Size the devices so that the output resistance is the same as that of an inverter with an nMOS W/L = 1 and pMOS W/L = 3.

(7 marks)

(b) Implement $F = A\overline{B}C + \overline{A}CD$ in CASCODE logic.

(3 marks)

(* You may assume true and complement signals are available for both sections (a) and (b))

4. Design a 2 →1 multiplexer and implement it in

(a) Dynamic domino logic.

(4 marks)

(b) Dynamic two-phase logic.

(4 marks)

(c) Discuss the merit of each design.

(2 marks)

(* Assume both true and complementary signals are available)

5. In order to drive a large capacitance C_L = 20 pF, from a minimum size inverter (with input capacitance, C_i = 10 fF) a designer decides to introduce a two-staged buffer. Assume that the propagation delay of a minimum size inverter is given by t_{po} = 70 psec. Also you may assume that the input capacitance of a gate is proportional to its size.

(a) Determine the sizing of the two additional buffer stages that will reduce the propagation delay as well as the value of the delay.

(7 marks)

(b) What is the minimum value of delay if this multistage buffer would have been designed for optimum delay?

(2 marks)

(c) What are the consequences of neglecting the drain capacitances?

(1 mark)

6. Describe what you understand by the following terms:

(a) Charge sharing
(b) Electromigration
(c) Body effect
(d) Channel Length modulation
(e) Lateral Diffusion

(2 marks each)

SPICE Transistor Parameters

Parameter	NMOS	PMOS	Units	Source	Description
VTO	0.7	-0.8	V	(1)	- zero bias threshold voltage
KP	40E-6	12E-6	(A/V^2)	(5)	- transconductance parameter
GAMMA	1.1	0.6	$(V^{0.5})$	(1)	- bulk threshold parameter
PHI	0.6	0.6	V	(3)	- surface potential
LAMBDA	0.01	0.03	1/V	(5)	- channel-length modulation
RD	(40)	(100)	ohms	(2)	- drain ohmic resistance (w=6u)
RS	(40)	(100)	ohms	(2)	- source ohmic resistance (")
CBD			F	(2)	- zero bias B-D junction cap.
CBS			F	(2)	- zero bias B-S junction cap.
IS			A	(2)	- bulk junction sat. current
PB	0.7	0.6	V	(1)	- bulk junction potential
CGSO	3.0E-10	2.5E-10	F/m	(1)	- G-S overlap capacitance
CGDO	3.0E-10	2.5E-10	F/m	(1)	- G-D overlap capacitance
CGBO	5.0E-10	5.0E-10	F/m	(1)	- G-bulk overlap capacitance
RSH	25	80	ohms/sq.	(1)	- diffusion sheet resistance
CJ	4.4E-4	1.5E-4	(F/m^2)	(1)	- zero bias bulk junction cap.
MJ	0.5	0.6	-	(1)	- bulk junction grading coef.
CJSW	4.0E-10	4.0E-10	F/m	(1)	- bulk junction sidewall cap.
MJSW	0.3	0.6	-	(1)	- sidewall cap. grading coef.
JS	1.0E-5	1.0E-5	(A/m^2)	(1)	- bulk junction sat. current
TOX	5.0E-8	5.0E-8	m	(1)	- oxide thickness
NSUB	1.7E16	5.0E15	$(1/cm^3)$	(1)	- substrate doping
NSS	0	0	$(1/cm^2)$	(3)	- surface state density
NFS	0	0	$(1/cm^2)$	(3)	- fast surface state density
TPG	1	1	-	(3)	- type of gate material
XJ	6.0E-7	5.0E-7	m	(1)	- metallurgical junction depth
LD	3.5E-7	2.5E-7	m	(1)	- lateral diffusion
UO	775	250	(cm^2/Vs)	(1)	- surface mobility
VMAX	1.0E5	0.7E5	m/s	(1)	- maximum drift velocity

SPICE Level 3 Parameters

Parameter	NMOS	PMOS	Units	Source	Description
THETA	0.11	0.13	1/V	(1)	- mobility modulation
KAPPA	1.0	1.0	-	(1)	- saturation field factor
ETA	0.05	0.3	-	(1)	- static feedback

Other Electrical Parameters

	Capacitance (pF/um^2)	Edge Component (pF/um)	Source
Gate (Cox)	6.9E-4	0.5E-4	(1)
Metal1 - Field	2.7E-5	0.4E-4	(1)
Metal1 - Poly	5.0E-5		(1)
Metal1 - Diffusion	5.0E-5		(1)
Poly - Field	6.0E-5	0.2E-4	(1)
Metal2 - Field	1.4E-5	2.0E-5	(4)
Metal2 - Diffusion	1.6E-5		(4)
Metal2 - Poly	2.0E-5		(4)
Metal2 - Metal1	2.5E-5		(4)
Capacitor P+ - Poly	6.9E-4	0.5E-4	(*)
(0.1%/V linearity)			(1)

Resistance	(ohms/sq.)	Source
N+ Diffusion	25	(1)
P+ Diffusion	80	(1)
N+ Poly	18	(5)
Capacitor P+	300	(1)
P-well	4K	(1)
Metal1	0.035	(4)
Metal2	0.030	(4)
3 x 3 metal1 - P+ Diffusion Contact	121	(5)
3 x 3 metal1 - N+ Diffusion Contact	44	(5)
3 x 3 Metal1 - N+ Poly Contact	25	(5)

Maximum operating voltage: 5 volts.

sources: (1) D. Smith of NTE, presented at CMC Workshop June 6-7, 1985.
(2) Calculated by SPICE: e.g. - RSH is used to calculate RD & RS.
(3) SPICE default.
(4) D. Smith of NTE, April 1986.
(5) Typical Measured DC result.
(*) Estimate - Capacitors assumed to be equal to gate capacitance.